

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte Furukawa et al.

Appeal No. _____

Appellants: Furukawa et al.
Serial No.: 10/777,576
Filed: February 12, 2004
Art Unit: 2811
Examiner: Ori Nadav
Title: **Vertical Carbon Nanotube Field Effect Transistors And Arrays**
Confirmation No.: 6152
Attorney Docket: ROC920030271US1

Cincinnati, OH 45202

June 4, 2007

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

BRIEF ON APPEAL

I hereby certify that this correspondence for Application No. 10/777,576 is being electronically transmitted to Technology Center 2811, via EFS-WEB, on June 4, 2007.

/William R. Allen/
William R. Allen, Reg. No. 48,389

June 4, 2007
Date

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BRIEF ON APPEAL

I. Real Party in Interest

The real party in interest is International Business Machines Corporation of Armonk, New York, which is the assignee of the present invention.

II. Related Appeals and Interferences

There are no related appeals or interferences known to Appellants or Appellants' legal representative that will directly effect or be directly effected by or have a bearing on the decision of the Board in the present appeal.

III. Status of the Claims

Claims 1, 3-13, 15-20, and 34-51 are rejected and claims 9-13, 20, 36, 38-42, and 49-51 are withdrawn, and claims 2, 14, and 21-33 are cancelled. Claims 1, 3-13, 15-20, and 34-51 are now on appeal.

IV. Status of Amendments

There have been no amendments filed subsequent to the final rejection dated March 26, 2007.

V. Summary of Claimed Subject Matter

Appellants' independent claim 1 is directed to a circuit comprising an interconnected plurality of semiconductor device structures (54) arranged in an array characterized by a plurality of rows and a plurality of columns. *See* Figs. 9A, 9B; page 5, line 1 to page 13, line 5. Each of the semiconductor device structures further comprises a gate electrode (25) including a vertical sidewall and a gate dielectric (38) disposed on the vertical sidewall. *See* page 8, lines 19-24; page 12, lines 16-23. At least one semiconducting carbon nanotube (42) extends substantially vertically between opposite first and second ends at a location adjacent to the vertical sidewall of the gate electrode (25). *See* page 10, lines 8-17; page 12, lines 16-23. A first contact (50) is electrically coupled with the first end of the at least one semiconducting carbon nanotube (42). *See* page 12, lines 4-23. A second contact (16) is electrically coupled with the second end of the at least one semiconducting carbon nanotube (42). *See* page 5, line 26 to page 6, line 4; page 8, lines 6-14; page 10, lines 8-17; page 12, lines 16-23.

Appellants' independent claim 43 is directed to a circuit comprising an interconnected plurality of semiconductor device structures (54). *See* Figs. 9A, 9B; page 5, line 1 to page 13, line 5. Each of the semiconductor device structures further comprises a gate electrode (25) including a vertical sidewall and a gate dielectric (38) disposed on the vertical sidewall. *See* page 8, lines 19-24; page 12, lines 16-23. At least one semiconducting carbon nanotube (42) extends substantially vertically between opposite first and second ends at a location adjacent to the vertical sidewall of the gate electrode (25). *See* page 10, lines 8-17; page

12, lines 16-23. A first contact (50) is electrically coupled with the first end of the at least one semiconducting carbon nanotube (42). *See* page 12, lines 4-23. A second contact (16) is electrically coupled with the second end of the at least one semiconducting carbon nanotube (42). *See* page 5, line 26 to page 6, line 4; page 8, lines 6-14; page 10, lines 8-17; page 12, lines 16-23.

VI. Grounds of Rejection to be Reviewed on Appeal

1. Claims 1, 3-8, 15-19, 34, 35, 37, 43-48, 52, and 53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,515,325 to Farnworth et al. in view of U.S. Publication No. 2004/0027889 to Occhipinti et al.

VII. Argument

Appellants respectfully submit that the Examiner's rejections of claims 1, 3-8, 15-19, 34, 35, 37, 43-48, 52, and 53 are not supported on the record, and that the rejections should be reversed.

A. *Claims 1, 3-8, 15-19, 34, 35, 37, 43-48, 52, and 53 were improperly rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,515,325 to Farnworth et al. in view of U.S. Publication No. 2004/0027889 to Occhipinti et al.*

The Examiner argues that claims 1, 3-8, 15-19, 34, 35, 37, 43-48, 52, and 53 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 6,515,325 to Farnworth et al. (hereinafter *Farnworth*) in view of U.S. Publication No. 2004/0027889 to Occhipinti et al. (hereinafter *Occhipinti*). A *prima facie* showing of obviousness requires that the Examiner establish that the differences between a claimed invention and the prior art "are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103(a). Such a showing requires that all claimed features be disclosed or suggested by the prior art. Such a showing also requires objective evidence of the suggestion, teaching or motivation to combine or modify prior art references, as "[c]ombining prior art references without evidence of such a suggestion, teaching or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior

art to defeat patentability -- the essence of hindsight." In re Dembiczak, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

Appellants respectfully submit that, in the instant case, the Examiner has failed to establish a *prima facie* case of obviousness as to any of the pending claims, and as such, the rejections should be reversed. Appellant will hereinafter address the various claims that are the subject of the Examiner's rejection in order.

Independent Claim 1

A person having ordinary skill in the art would understand that the structure shown in Figure 1 of *Farnworth*, even with the modification proposed by the Examiner, fails to disclose or suggest a plurality of nanotubes and that each of the nanotubes includes “a first end electrically coupled with said source region” and “a second end electrically coupled with said drain region.”

According to MPEP § 2111.01, words of the claim must be given their plain (i.e., ordinary and customary) meaning unless a clear definition is provided in the specification. The plain meaning is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application. The plain meaning of the term “end” would have been “either extremity of something that has a length.” See, e.g., The American Heritage Dictionary, 3rd Ed., p. 453. “Extremity” may be defined as “the outermost or farthest point or portion.” See, e.g., The American Heritage Dictionary, 3rd Ed., p. 486.

The disclosure in *Farnworth* is subject to multiple reasonable interpretations regarding the shape of nanotube (22) shown in Figure 1. Under one reasonable interpretation, the nanotube (22) in *Farnworth* appears to have an inverted U-shape based upon the lead line for reference numeral (22) in Figure 1. Based on the plain meaning of the term “end” and the definition of “extremity” supplied above, a person having ordinary skill in the art would comprehend that a first “end” of the U-shaped nanotube (22) in *Farnworth* is electrically coupled with a first contact represented by the source (17) of device (10). However, the second “end” of the U-shaped nanotube (22) is not electrically coupled with the second contact represented by the drain (21) of device (10). Instead, the first and second ends (i.e., the lengthwise extremities) of the nanotube (22) are both electrically coupled with the first contact represented by source (17) of device (10).

Under an alternative reasonable interpretation, the nanotube (22) shown in Figure 1 (and in Figures 2C-I) of *Farnworth* may be construed to have the shape of a right circular cylinder labeled with reference numeral 30 (although Appellants cannot find the element labeled with reference numeral 30 in the written description of *Farnworth*). Based on the plain meaning of the term “end” and the definition of “extremity” supplied above, a person having ordinary skill in the art would comprehend that a first “end” of the cylindrical nanotube (22, 30) in *Farnworth* is electrically coupled with a first contact represented by the source (17) of device (10). However, the second “end” of the nanotube (22) is not electrically coupled with the second contact represented by the drain (21) of device (10). Instead, the second end (i.e., one of the lengthwise extremities) of the nanotube (22) in *Farnworth* projects far above the vertical level of the second contact represented by the drain (21) of device (10).

The disclosure in *Farnworth* is consistent with the Appellants’ construction of the term “end”. Specifically, *Farnworth* describes in the “Summary” section at column 1, lines 50-60 that the nanotube can form a via between first and second trace layers in which “a lower end [of the nanotube] is connected to the first trace layer” and “[a] second trace layer is electrically connected to an upper end of the nanotube.” In the “Detailed Description” section of *Farnworth* and in conjunction with Figure 3, *Farnworth* describes that the nanotube (22) is connected to the first trace layer (54) and that a second trace layer (60) covers an upper portion of the nanotube (22). *See* column 5, line 57-column 6, line 3. This constitutes the only related discussion in the “Detailed Description” section of a “via” embodiment and, hence, correlates with the discussion in the “Summary” section of *Farnworth*. In Figure 3 and consistent with Appellant’s definition of the term “end”, the opposite ends of the nanotube (22) are electrically coupled with the traces (52, 60), respectively. Hence, a person having ordinary skill in the art would recognize from the disclosure in *Farnworth* that the “ends” of the nanotube (22) represent “either extremity of something that has a length” consistent with the plain meaning of the term “end”.

Occhipinti fails to remedy this deficiency in the disclosure of *Farnworth*. Specifically, *Occhipinti* fails to disclose a plurality of nanotubes and that each of the nanotubes has “a first end electrically coupled with said source region” and “a second end electrically coupled with said drain region.”

To establish a *prima facie* case of obviousness, the prior art references must teach or

suggest all the claim limitations. *See* MPEP § 2143. Because *Farnworth* and *Occhipinti* fail to disclose “a plurality of nanotubes and that each of the nanotubes includes “a first end electrically coupled with said source region” and “a second end electrically coupled with said drain region” as set forth in Appellants’ independent claim 1, reversal of the Examiner's rejection of claim 1 under 35 U.S.C. § 103(a) is therefore respectfully requested for this reason alone.

The rejection of Appellants’ independent claim 1 should be reversed for at least an additional reason.

Specifically, a person having ordinary skill in the art would not have combined *Occhipinti* with *Farnworth* because there is no suggestion or reason to make the combination. The Examiner relies on *Occhipinti* to remedy deficiencies in *Farnworth* and contends that *Occhipinti* discloses that “a memory device conventionally uses an array characterized by a plurality of rows and a plurality of columns (paragraph [0010]).” However, paragraph [0010] of *Occhipinti* fails to disclose how device structures in a memory device that is not “conventional” could use such an array. Specifically, paragraph [0010] of *Occhipinti* fails to disclose or suggest how the rows and columns of the array would be arranged for the device structure disclosed in *Farnworth* that include nanotubes having first and second contacts in the form of conductive rings that are not located at the ends of the nanotubes. Paragraph [0010] of *Occhipinti* also fails to disclose or suggest how connections for the rows and columns would be established for the device structure disclosed in *Farnworth* that include nanotubes having first and second contacts in the form of conductive rings that are not located at the ends of the nanotubes. A person having ordinary skill in the art would have had to somehow resolve these deficiencies of paragraph [0010] in *Occhipinti* in order to modify *Farnworth* based upon *Occhipinti*.

According to MPEP § 2143, the prior art can be modified or combined to reject claims as *prima facie* obvious as long as there is a reasonable expectation of success. In this instance, a person having ordinary skill in the art would not have appreciated from the disclosure found at paragraph [0010] of *Occhipinti* that a reasonable expectation of success exists to combine *Occhipinti* with *Farnworth* if the device structures are not conventional but instead are configured as disclosed in *Farnworth* with nanotubes having source and drain connections in the form of rings that are not located at the ends of the nanotubes.

In the absence of a proper suggestion or motivation to combine *Occhipinti* with

Farnworth, the Examiner has failed to support *prima facie* obviousness under MPEP § 2143. For this additional reason, reversal of the Examiner's rejection of claim 1 under 35 U.S.C. § 103(a) is therefore respectfully requested.

Dependent Claim 3

Claim 3 is not argued separately.

Dependent Claim 4

For at least the same reasons as discussed above in connection with claim 1, the Examiner has failed to establish that dependent claim 4 is obvious over the combination of *Farnworth* and *Occhipinti*. Consequently, the rejection of dependent claim 4 should be reversed.

The rejection of dependent claim 4 should be reversed for additional reasons. On page 3 of the March 26, 2007 Office Action, the Examiner refers Appellants to Figure 2I of *Farnworth* as disclosing “a plurality of semiconducting carbon nanotubes extending vertically at a plurality of locations adjacent to said vertical sidewall of said gate electrode.” Appellants agree that Figure 2I of *Farnworth* discloses multiple carbon nanotubes (22). However, each of these carbon nanotubes (22) includes a separate gate electrode ring (46). As a result, the plurality of carbon nanotubes (22) in Figure 2I of *Farnworth* are not adjacent to a vertical sidewall of the same gate electrode, as required by claim 4. *Occhipinti* fails to remedy this deficiency of *Farnworth*.

To establish a *prima facie* case of obviousness, the prior art references must teach or suggest all the claim limitations. See MPEP § 2143. Because of the aforementioned deficiency in the combined disclosure of *Farnworth* and *Occhipinti*, reversal of the Examiner's rejection of claim 4 under 35 U.S.C. § 103(a) is therefore respectfully requested for this additional reason.

Dependent Claim 5

Claim 5 is not argued separately.

Dependent Claim 6

For at least the same reasons as discussed above in connection with claim 1, the Examiner has failed to establish that dependent claim 6 is obvious over the combination of *Farnworth* and *Occhipinti*. Consequently, the rejection of dependent claim 6 should be reversed.

The rejection of dependent claim 6 should be reversed for additional reasons. On page 3 of the March 26, 2007 Office Action, the Examiner fails to direct the Appellants to any specific disclosure in *Farnworth*, or otherwise, that discloses “said first end of said at least one semiconducting carbon nanotube incorporates an electrical-conductivity enhancing substance”, as required by claim 6. *Occhipinti* fails to remedy this deficiency of *Farnworth*.

To establish a *prima facie* case of obviousness, the prior art references must teach or suggest all the claim limitations. See MPEP § 2143. Because of the aforementioned deficiency in the combined disclosure of *Farnworth* and *Occhipinti*, reversal of the Examiner's rejection of claim 6 under 35 U.S.C. § 103(a) is therefore respectfully requested for this additional reason.

Dependent Claims 7, 8, and 15-18

Claims 7, 8, and 15-18, which depend either directly or indirectly from independent claim 1, are not argued separately.

Dependent Claim 19

For at least the same reasons as discussed above in connection with claim 1, the Examiner has failed to establish that dependent claim 19 is obvious over the combination of *Farnworth* and *Occhipinti*. Consequently, the rejection of dependent claim 19 should be reversed.

The rejection of dependent claim 19 should be reversed for additional reasons. On page 5 of the March 26, 2007 Office Action, the Examiner states that “it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a space ranging from about 20 percent to about 50 percent of said surface area in prior art’s device in order to reduce the size of the device and by optimizing the characteristics of the device”. The rationales offered by the Examiner for supplying this disclosure, which the Examiner admits is absent in *Farnworth* (and *Occhipinti*) are strained. Appellants fail to comprehend how requiring the dielectric-filled space between the device structures to be in the range of about 20 percent to about 50 percent of the total surface area can reduce the size of the device structures, as contended by the Examiner. The area between device structures that is filled by a dielectric is independent of the dimensions of the features of the individual device structures. Appellants also fail to comprehend how requiring the dielectric-filled space between the device structures to be in the range of about 20 percent to about 50 percent of the total surface area can optimize the characteristics of the device structures, as contended by the Examiner. The area between device structures that is filled by a dielectric is independent of the device performance.

To establish a *prima facie* case of obviousness, the prior art references must teach or suggest all the claim limitations. See MPEP § 2143. Because of the aforementioned deficiency in the combined disclosure of *Farnworth* and *Occhipinti*, reversal of the Examiner’s rejection of claim 19 under 35 U.S.C. § 103(a) is therefore respectfully requested for this additional reason.

Dependent Claims 34, 35, and 37

Claims 34, 35, and 37, which depend either directly or indirectly from independent claim 1, are not argued separately.

Independent Claim 43

Independent claim 43 is not argued separately. However, for at least the same reasons as discussed above in connection with claim 1, the Examiner has failed to establish that independent claim 43 is obvious over the combination of *Farnworth* and *Occhipinti*. Consequently, the rejection of independent claim 43 should be reversed.

Dependent Claim 44

Claim 44 is not argued separately.

Dependent Claim 45

For at least the same reasons as discussed above in connection with claim 43, the Examiner has failed to establish that dependent claim 45 is obvious over the combination of *Farnworth* and *Occhipinti*. Appellants also incorporate by reference the reasons set forth hereinabove with regard to dependent claim 4. Consequently, the rejection of dependent claim 45 should be reversed for at least these reasons.

Dependent Claims 46-48

Claims 46-48 are not argued separately.

Dependent Claim 52

For at least the same reasons as discussed above in connection with claim 43, the Examiner has failed to establish that dependent claim 52 is obvious over the combination of *Farnworth* and *Occhipinti*. Appellants also incorporate by reference the reasons set forth hereinabove with regard to dependent claim 19. Consequently, the rejection of dependent claim 52 should be reversed for at least these reasons.

Dependent Claim 53

Claim 53 is not argued separately.

VIII. Conclusion

In conclusion, Appellants respectfully request that the Board reverse the Examiner's rejections of claims 1, 3-8, 15-19, 34, 35, 37, 43-48, 52, and 53, and that the application be passed to issue. If there are any questions regarding the foregoing, please contact the

undersigned. Moreover, if any other charges or credits are necessary to complete this communication, please apply them to Deposit Account 23-3000.

Respectfully submitted,
WOOD, HERRON & EVANS, L.L.P.

Date: June 4, 2007

By: /William R. Allen/
William R. Allen, Reg. No. 48,389

2700 Carew Tower
441 Vine Street
Cincinnati, OH 45202
(513) 241-2324

APPENDIX OF CLAIMS

1. (Previously Presented) A circuit comprising:
an interconnected plurality of semiconductor device structures arranged in an array characterized by a plurality of rows and a plurality of columns, each of said semiconductor device structures further comprising a gate electrode including a vertical sidewall and a gate dielectric disposed on the vertical sidewall, at least one semiconducting carbon nanotube extending substantially vertically between opposite first and second ends at a location adjacent to said vertical sidewall of said gate electrode, a first contact electrically coupled with said first end of said at least one semiconducting carbon nanotube, and a second contact electrically coupled with said second end of said at least one semiconducting carbon nanotube.
2. (Cancelled)
3. (Previously Presented) The circuit of claim 1 wherein said at least one semiconducting carbon nanotube is a single-wall semiconducting carbon nanotube.
4. (Previously Presented) The circuit of claim 1 wherein each of said plurality of semiconductor device structures further comprises:
a plurality of semiconducting carbon nanotubes extending vertically at a plurality of locations adjacent to said vertical sidewall of said gate electrode.
5. (Previously Presented) The circuit of claim 1 wherein said first contact includes a catalyst pad characterized by a catalyst material effective for growing said at least one semiconducting carbon nanotube.
6. (Previously Presented) The circuit of claim 5 wherein said first end of said at least one semiconducting carbon nanotube incorporates an electrical-conductivity enhancing substance diffused from said catalyst pad into said first end during growth.

7. (Previously Presented) The circuit of claim 1 wherein each of said plurality of semiconductor device structures further comprises:

an insulating layer disposed between said first contact and said gate electrode for electrically isolating said first contact from said gate electrode.

8. (Previously Presented) The circuit of claim 1 wherein each of said semiconductor device structures further comprises:

an insulating layer disposed between said second contact and said gate electrode for electrically isolating said second contact from said gate electrode.

9. (Withdrawn) The circuit of claim 1 wherein each of said plurality of semiconductor device structures further comprises:

a third contact; and

at least one electrically-conducting carbon nanotube electrically coupling said gate electrode with said third contact.

10. (Withdrawn) The circuit of claim 1 wherein said second contact includes a vertically-extending metal post electrically coupled with said second end of said at least one semiconducting carbon nanotube.

11. (Withdrawn) The circuit of claim 10 wherein said second contact includes a conductive layer extending horizontally beneath said gate electrode for electrically coupling said catalyst pad with said metal post.

12. (Withdrawn) The circuit of claim 1 wherein said second contact includes at least one electrically conducting carbon nanotube extending substantially vertically and electrically coupled with said second end of said at least one semiconducting carbon nanotube.

13. (Withdrawn) The circuit of claim 12 wherein said second contact includes a conductive layer extending horizontally beneath said gate electrode for electrically coupling said second end

of said at least one semiconducting carbon nanotube with said at least one electrically conducting carbon nanotube.

14. (Cancelled)

15. (Previously Presented) The circuit of claim 1 wherein said plurality of semiconductor device structures are interconnected as a memory circuit.

16. (Previously Presented) The circuit of claim 15 further comprising:

a plurality of word lines each electrically interconnecting said gate electrode of each of said plurality of semiconductor device structures located in a corresponding one of said plurality of rows of said array; and

a plurality of bit lines each electrically interconnecting said second contact of each of said plurality of semiconductor device structures located in a corresponding one of said plurality of columns of said array.

17. (Previously Presented) The circuit of claim 16 wherein each of said plurality of word lines comprises said gate electrode of each of said plurality of semiconductor device structures located in said corresponding one of said plurality of rows of said array.

18. (Previously Presented) The circuit of claim 16 wherein each of said plurality of bit lines comprises a conductive stripe electrically coupling said source of each of said plurality of semiconductor device structures located in a corresponding one of said plurality of rows of said array.

19. (Previously Presented) The circuit of claim 1 further comprising:

a substrate carrying said plurality of semiconductor device structures and characterized by a surface area viewed vertical to the substrate, said plurality of semiconductor device structures separated by a space filled by a dielectric material, and said space ranging from about 20 percent to about 50 percent of said surface area.

20. (Withdrawn) The circuit of claim 1 wherein said plurality of semiconductor device structures are interconnected as a logic circuit.

21-33. (Cancelled)

34. (Previously Presented) The circuit of claim 5 wherein said catalyst pad further comprises nanocrystals of the catalyst material.

35. (Previously Presented) The circuit of claim 13 wherein each of said semiconductor device structures further comprises:

a catalyst pad electrically coupling said electrically conducting carbon nanotube with said conductive layer, said catalyst pad participating in the synthesis of said electrically conducting carbon nanotube.

36. (Withdrawn) The circuit of claim 35 wherein said catalyst pad further comprises nanocrystals of the catalyst material.

37. (Previously Presented) The circuit of claim 1 wherein each of said semiconductor device structures further comprises:

a capacitor electrically coupled with said first contact.

38. (Withdrawn) The circuit of claim 11 further comprising:

an insulating layer positioned between said conductive layer and said gate electrode, said insulating layer electrically isolating said gate electrode from said conductive layer.

39. (Withdrawn) The circuit of claim 11 further comprising:

a substrate carrying said plurality of semiconductor device structures, said conductive layer being arranged vertically between said gate electrode and said substrate.

40. (Withdrawn) The circuit of claim 13 further comprising:
an insulating layer positioned between said conductive layer and said gate electrode, said insulating layer electrically isolating said gate electrode from said conductive layer.
41. (Withdrawn) The circuit of claim 13 further comprising:
a substrate carrying said plurality of semiconductor device structures, said conductive layer being arranged vertically between said gate electrode and said substrate.
42. (Withdrawn) The circuit of claim 9 wherein each of said semiconductor device structures further comprises:
a catalyst pad electrically coupling said electrically conducting carbon nanotube with said gate electrode, said catalyst pad participating in the synthesis of said electrically conducting carbon nanotube.
43. (Previously Presented) A circuit comprising:
an interconnected plurality of semiconductor device structures, each of said plurality of semiconductor device structures further comprising a gate electrode including a vertical sidewall and a gate dielectric disposed on the vertical sidewall, at least one semiconducting carbon nanotube extending substantially vertically between opposite first and second ends at a location adjacent to said vertical sidewall of said gate electrode, a first contact electrically coupled with said first end of said at least one semiconducting carbon nanotube, and a second contact electrically coupled with said second end of said at least one semiconducting carbon nanotube.
44. (Previously Presented) The circuit of claim 43 wherein said at least one semiconducting carbon nanotube is a single-wall semiconducting carbon nanotube.
45. (Previously Presented) The circuit of claim 43 wherein each of said plurality of semiconductor device structures further comprises:
a plurality of semiconducting carbon nanotubes extending vertically at a plurality of locations adjacent to said vertical sidewall of said gate electrode.

46. (Previously Presented) The circuit of claim 43 wherein said first contact includes a catalyst pad characterized by a catalyst material effective for growing said at least one semiconducting carbon nanotube.

47. (Previously Presented) The circuit of claim 43 wherein each of said plurality of semiconductor device structures further comprises:

an insulating layer disposed between said first contact and said gate electrode for electrically isolating said first contact from said gate electrode.

48. (Previously Presented) The circuit of claim 43 wherein each of said plurality of semiconductor device structures further comprises:

an insulating layer disposed between said second contact and said gate electrode for electrically isolating said second contact from said gate electrode.

49. (Withdrawn) The circuit of claim 43 wherein each of said plurality of semiconductor device structures further comprises:

a third contact; and

at least one electrically conducting carbon nanotube electrically coupling said gate electrode with said third contact.

50. (Withdrawn) The circuit of claim 43 wherein said second contact includes a vertically-extending metal post electrically coupled with said second end of said at least one semiconducting carbon nanotube.

51. (Withdrawn) The circuit of claim 43 wherein said second contact includes at least one electrically conducting carbon nanotube extending substantially vertically and electrically coupled with said second end of said at least one semiconducting carbon nanotube.

52. (Previously Presented) The circuit of claim 43 further comprising:
a substrate carrying said plurality of semiconductor device structures and characterized by a surface area viewed vertical to the substrate, said plurality of semiconductor device structures separated by a space filled by a dielectric material, and said space ranging from about 20 percent to about 50 percent of said surface area.
53. (Previously Presented) The circuit of claim 43 wherein each of said semiconductor device structures further comprises:
a capacitor electrically coupled with said first contact.

APPENDIX OF EVIDENCE

(None)

APPENDIX OF RELATED PROCEEDINGS

(None)